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## OBJECTIVE

Research and/or Engineering on microelectronics or semiconductor industry, on design and technology of semiconductor device and circuit.

## EDUCATION

**Ph.D., Electrical & Computer Engineering.** Expected graduation in May 1998. GPA 4.0. School of Information Technology & Engineering (SITE), George Mason University, Fairfax, Virginia. Ph.D. research on physics, design and technology of semiconductor devices and circuits, esp. SOI MOSFET & ULSI.

**M.S., Electrical Engineering.** December 1987. GPA 3.2. Institute of Microelectronics, Tsinghua University, Beijing, China. Research on VLSI processes.

**B.Sc., Electrical Engineering.** July 1985. GPA 3.3. Tsinghua University, Beijing, China.

## PROFESSIONAL EXPERIENCE

**Process Engineer,** Singapore Technology, Chartered Semiconductor Manufacturing. May 1992-December 1992. Process integration and semiconductor chip manufacturing of 0.8um VLSI technology.

**Research Associate,** Institute of Semiconductors, Chinese Academy of Sciences, China. December 1987-January 1991. Physics of superconductor devices and III-V compound semiconductors.

**Chief Engineer,** Haida Corporation, Beijing, China. January 1991-May 1992. Sale and customer service of computer hardware and software.

## PROFESSIONAL SKILLS

### Semiconductor Simulation:

4 years' experience of using semiconductor simulation tools, including process simulation--SUPREM, device simulation--PISCES, and circuit simulation--SPICE.

### Semiconductor Characterization:

Comprehensive measurements on semiconductor transistors (esp. on MOSFETs and SOI MOSFETs). I-V characterization and hot carrier degradation test, using HP 4145 Semiconductor Parameter Analyzer together with the Pulse Generators, PCs...

### Computer Skills:

- Operating System: UNIX, DOS, Win95, and HP
- Programming Language and Software Utility: C(C++), HP BASIC, and HTML. Microsoft Office and NETSCAPE. QuatroPro, Lotus, Matlab, PaintShop...
- Computer Aided Measurement: Interface language programming on electronic equipment like HP4145 and HP Pulse Generator by PC.

## AWARDS AND HONORS

1995, 1997 Fellowship in George Mason University

## PROFESSIONAL MEMBERSHIP

IEEE Student Membership from 1992

Who's Who in Science and Engineering from 1998

## PUBLICATIONS

See separated

## REFERENCES

Prof. D.E. Ioannou, Department of Electrical & Computer Engineering, George Mason University. (703) 993-1580.

Prof. R.V. Mulpuri, Department of Electrical & Computer Engineering, George Mason University. (703) 993-1612.

Prof. A. Sofer, School of Information Technology and Engineering, George Mason University. (703) 993-1692.

Prof. D.A. Schum, School of Information Technology and Engineering, George Mason University. (703) 993-1694.

## Publications

1. Franklin L. Duan, Dimitris E. Ioannou, Shankar P. Sinha, and Frederick T. Brady, "LDD Design Tradeoffs for Self Latch-Up and Hot Carrier Degradation Control in Accumulation Mode FD SOI MOSFET's", *IEEE Transactions on Electron Devices*, vol. 44, pp.972-977, 1997.
2. F.L. Duan, X.Zhao, D.E. Ioannou, H.L. Hughes and S.T. Liu, "Detrimental Edge Effects on the Floating Body Phenomena in SOI MOSFETs", *Symposium of 192nd International Meeting of the Electrochemical Society, Inc.*, pp.239-245, 1997.
3. Franklin L. Duan and Dimitris E. Ioannou, "Design and Analysis of a Novel Mixed Accumulation/Inversion Mode FD SOI MOSFET", *1997 IEEE International SOI Conference Proceedings*, pp.100-101, 1997.
4. Franklin L. Duan, Dimitris E. Ioannou, Harold L. Hughes and Mike Liu, "Channel Coupling Imposed Tradeoffs Between Hot Carrier Degradation and Single Transistor Latch-Up in FD SOI MOSFET's", *IEEE International Reliability Physics Symposium*, pp.194-202, 1998.
5. Dimitris E. Ioannou, Franklin L. Duan, Shankar P. Sinha, and Andrej Zaleski, "Opposite-Channel-Based Injection (OCBI) of Hot-Carriers in SOI MOSFET's: Physics and Applications", *IEEE Transaction on Electron Devices*, vol.45, May 1998.
6. D.E. Ioannou, F.L. Duan, and X. Zhao, "SIMOX Substrate and MOSFET's for Enhanced Reliability and Performance", *1997 International Semiconductor Device Research Symposium*, pp.627-630, 1997.
7. Dimitris E. Ioannou, Franklin L. Duan, Williams C. Jenkins, and Harold L. Hughes, "Channel Coupling Imposed Tradeoffs on Fully-Depleted (FD) SOI MOSFET's", *submitted to ESSDREC'98*.
8. X. Zhao F.L. Duan, A. Thanailakis, D.E. Ioannou, R.K. Lawrence, and H.L. Hughes, "Hole Trap Investigation in Supplemental Oxygen SIMOX Wafers by Opposite Channel Based Charge Injection", *1997 IEEE International SOI Conference Proceedings*, pp.116-117, 1997.
9. Shankar P. Sinha, Franklin L. Duan, Dimitris E. Ioannou, William C. Jenkins, and Harold L. Hughes, "Time Dependence Power Laws of Hot Carrier Degradation in SOI MOSFET's", *1996 IEEE International SOI Conference Proceedings*, pp.18-19, 1996.
10. S. P. Sinha, F.L. Duan, D.E. Ioannou, William C. Jenkins, Harold L. Hughes, and M.S. Liu, "Hot Carrier Degradation of Fully Depleted SIMOX MOSFET's", *Proceedings of the 7th International Symposium On Silicon-On-Insulator Technology and Devices*, pp.324-329, 1996.